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Substitute for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<i>Complete if Known</i>	
				Application Number	09/511,737
				Filing Date	February 24, 2000
				First Named Inventor	YELLIN, Daniel
				Group Art Unit	2124
				Examiner Name	MAI, Tan V.
Sheet	1	of	2	Attorney Docket Number	P-5332-US

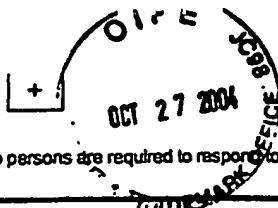
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<sup>1</sup> Unique citation designation number. <sup>2</sup> See attached Kinds of U.S. Patent Documents. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST 3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached

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PTO/SB/08A (10-96)  
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Sheet 2 of 2	Attorney Docket Number	P-5332-US	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (where appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
man	B	UMING KO et al., "A Self-Timed Method to Minimize Spurious Transitions in Low Power CMOS Circuits", Low Power Electronics, 1994, Digest of Technical Papers, IEEE Symposium, San Diego CA, USA, 10 OCT 1994, pp. 82-83	<input type="checkbox"/>
↓	C	Vivek Tiwari, "Guarded evaluation: pushing power management to logic synthesis/design", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 17, No. 10, 10 OCT 1998, pp. 1051-1060	<input type="checkbox"/>
✓	D	Supplementary Search Report for EP 01 80 6088	<input type="checkbox"/>
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